

## CLAIMS

I claim:

1. A buffer system comprising:

a buffer that is configured to be accessed via a first pointer and a second pointer, and

a buffer manager that is configured to limit the second pointer, based on the first pointer,

wherein

the first pointer is configured provide a sequential block-level access to the buffer, and an independent within-block access to the buffer, and

the buffer manager is configured to limit the second pointer to a limit value that corresponds to the sequential block-level access of the first pointer.

2. The buffer system of claim 1, wherein

the buffer manager is further configured to reset the limit value to correspond to the first pointer, when the independent within-block access to the buffer corresponds to the sequential block-level access to the buffer.

3. The buffer system of claim 1, wherein

the first pointer includes a block address and an offset address, and

the buffer manager is configured to:

set the limit value to correspond to the block address when the independent within-block access to the buffer does not correspond to the sequential block-level access, and

set the limit value to correspond to a combination of the block address and the offset address when the independent within-block access to the buffer corresponds to the sequential block-level access.

4. The buffer system of claim 1, wherein

the first pointer and the second pointer correspond to:

a write-pointer for writing data to the buffer, and

a read-pointer for reading data from the buffer.

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5. The buffer system of claim 1, wherein

the first pointer includes a block address and an offset address,

the block address corresponding to the sequential block-level access, and

the offset address corresponding to the independent within-block access; and

the buffer manager is further configured to minimize changes to the offset access  
between sequential block-level accesses.

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6. The buffer system of claim 1, wherein

the buffer manager is further configured to advance the limit value prior to a completion  
of a block-level access of the buffer via the first pointer.

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7. The buffer system of claim 6, wherein

the buffer manager is further configured to communicate the limit value via a gray-code  
sequence corresponding to the advance of the limit value.

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8. The buffer system of claim 1, wherein

the buffer manager is further configured to communicate the limit value via a gray-code  
sequence.

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9. A buffer management system for controlling access to a buffer, comprising  
a buffer manager that is configured to assert a wrap signal when a first access to the  
buffer is non-sequential, and is further configured to limit a second access to the buffer in  
dependence upon the wrap signal.

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10. The buffer management system of claim 9, wherein

the first access to the buffer includes an access that is based on a block address and an  
offset address, and

10 the second access to the buffer is limited to the block address when the wrap signal is  
asserted, and is limited to a combination of the block address and the offset address when the  
wrap signal is deasserted.

11. The buffer management system of claim 10, wherein

a change of limit of the second access is communicated via a gray-code sequence.

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12. The buffer management system of claim 10, wherein

the buffer manager is further configured to assert an idle signal when the first access to  
the buffer terminates, and

20 the second access to the buffer is further limited to the block address when the idle signal  
is asserted.

13. The buffer management system of claim 9, wherein

the first access and the second access correspond to:

a write-access to the buffer, and

25 a read-access to the buffer.

14. A method of controlling access to a buffer comprising:

determining a block address and an offset address corresponding to a first access to the buffer,

determining when the offset address is non-sequential relative to the block address, and

limiting a second access to the buffer to the block address when the offset address is non-sequential.

15. The method of claim 14, further including:

determining when the offset address is sequential relative to the block address, and

limiting the second access to the buffer to a combination of the block address and the offset address when the offset address is sequential.

16. The method of claim 14, wherein

limiting the second access includes determining a gray-code sequence corresponding to a change in the block address.